Kumudha KN

Personal Details

Current Position:	Staff Software Engineer, Codeplay Software
Locale:	Edinburgh, UK (Citizenship: Indian)
Date of Birth:	4 December 1990
Portfolio / Blog:	https://kumudhan.github.io/
email:	kumudhakn@gmail.com

Work Experience

September 2019 to Current — Staff Software Engineer at Codeplay Software, Edinburgh
AI/DNN Compilation and Performance Engineering. SYCL, CUDA, OpenCL

July 2018 to July 2019 (1 year, 1 month) — Senior Software Engineer at Samsung Research India, Bangalore
IoT Division. Tizen studio infrastructure development and maintenance

June 2012 to July 2015 (3 years 1 month) — Technology Analyst at Goldman Sachs, Bangalore, India
Investment Banking Division, Technology
Application Infrastructure Team. Focused on building and standardizing frameworks in C# .NET and Java for applications developed in the division

June 2011 to August 2011 (3 months) — Summer Analyst at Goldman Sachs, Bangalore, India
Re-architected and enhanced the UI of a Reporting application.
Received Pre-Placement offer for "*distinctive*" Performance

Education

June 2018 — Indian Institute Of Science, Bangalore, India
M.Sc Engineering | Dept of Computer Science and Automation
Research: *High Performance Computing & Compilers* | Advisor: Uday Reddy
GPA: 7.0/8.0 | List of Courses

May 2012 — M S Ramaiah Institute of Technology, Bangalore, India
Bachelor of Engineering | Dept of Computer Science and Engineering
GPA: 9.92/10.0 | List of Courses

June 2008 — Vidya Mandir Pre-University College, Malleshwaram, Bangalore, India
Karnataka Pre-University Course (PUC)
Percentage: 90.83 (PCM: 95.33) | List of Courses

July 2006 — B P Indian Public School, Malleshwaram, Bangalore, India
ICSE 10th Percentage: 90.16

Publications

A Practical Tile Size Selection Model for Affine Loop Nests
Kumudha Naraimshan, Aravind Acharya, Abhinav Baid, Uday Bondhugula
ACM International Conference on Supercomputing (ICS) 2021

Cross-Platform Performance Portability of DNN Models using SYCL
Mehdi Goli, Kumudha Naraimshan, Ruyman Reyes et. al.
Performance, Portability, and Productivity in HPC Forum (P3HPC) @ Supercomputing (SC) 2020

Optimizing Geometric Multigrid Method Computation using a DSL Approach
Vinay Vasista, Kumudha KN, Siddharth Bhat, Uday Bondhugula
SuperComputing (SC) 2017, The Intl. Conf. for High Performance Computing, Networking, Storage and Analysis.

An Empirical Comparative Study and Optimization of the Hadoop Scheduler
Jayalakshmi DS, Kumudha KN, Tejala T, Veena Pilli
International Conference on Emerging Trends in Electrical, Electronics and Communication Technologies
ICECIT, 2012, pgs 350-356,2012

Software & Hardware Proficiency

SOFTWARE

- *Compiler Tools:* isl, Barvinok, Pluto
- *DNN Frameworks:* Caffe, Latte
- *Architectural Simulators:* gem5-gpu, gem5
- *Development Platforms:* Eclipse, VI / VIM, Visual Studio, gedit, TexStudio
- *Web Technology:* HTML5, CSS3, AngularJS, ExtJS, XML
- *Operating Systems:* Linux (CentOS, Ubuntu), Windows
- *Libraries:* CUDA, OpenMP, OpenGL
- *Tools:* LaTeX , git, svn, gdb, Intel VTune
- *Database:* MySQL, Oracle, SQL Server
- *Programming Languages:* C, C++, Python, Java, Hibernate, Spring, C#, .NET, ASP, WPF, WCF, shell scripting

HARDWARE

- Programming and Architecture of Accelerators
  Intel MIC (XeonPhi KNC) and NVIDIA Fermi and Volta GPGPUs, Google TPU
- Micro-Architecture and Efficient Programming of Modern x86 CPUs
  Intel Xeon (SandyBridge, IvyBridge, Haswell)
- 8051 based Micro-controller Programming

Projects

Projects at INDIAN INSTITUTE OF SCIENCE

Optimizing Geometric Multigrid Method Computation using a DSL Approach [SC 2017]

The Geometric Multigrid (GMG) method is widely used in numerical analysis to accelerate the convergence of partial differential equations solvers using a hierarchy of grid discretizations. However, multiple grid sizes and recursive expression of multigrid cycles make the task of program optimization tedious. A high-level language that aids domain experts (productivity) for GMG with effective optimization and parallelization support (performance) is thus valuable. Technologies used: C/C++, python and pgfplot.

Optimizing Dense Matrix Computations with Polymage [Masters Thesis]

Matrix computations constitute an important part in domains like digital signal processing, scientific computing, media processing and many others. A Domain specific language(DSL) which provides high performance and aids in productivity is thus very useful. Polymage is a DSL which accepts specification in python based format and generates optimized C/C++ code after performing transformations on the input specification. Technologies used: C/C++, python and pgfplot.

Evaluating Performance Overheads in Program execution of Scripting Languages under Virtual Machine Environment

Scripting languages are widely used among statisticians and data miners for developing statistical software and data analysis. They are run on virtual machines which are either interpreted or compiled just-in-time during execution. McVM is a virtual machine implemented in C/C++ which implements a significant subset of the MATLAB language.This work evaluates the overheads associated with the execution of MATLAB scripting languages under McVM virtual machine environment. Technologies used: C/C++ and Intel PIN tool.

Projects

Parallelize and optimize the CAFFE DNN framework on a multicore CPU

CAFFE is one of the early frameworks for deep neural networks written in C++. CAFFE accepts a configuration in protobuf containing the neural network topology and can perform training, testing and inference. CAFFE has support for executing on both CPUs and GPUs. We optimize the CPU version of Caffe to improve its performance using loop transforms for extracting parallelism. Technology used: C/C++ and Intel vTune profiler.

Optimizations for Image Processing Pipeline

Hand optimization of image processing pipelines like unsharp mask, harris corner detection, max_filter, etc on multi-core CPUs. These optimizations included loop permutation, tiling for cache locality and parallelism and were done in C/C++. Technology used: C/C++ and Intel vTune profiler.

Integrated Heterogeneous System (IHS) Architecture with shared die-stacked DRAM Cache

Modern processors chips integrate multi-core CPUs and general purpose GPUs on the same die. These IHS processors have high bandwidth requirement and large working sets. Die-stacking technology allows high bandwidth and large capacity DRAM to be integrated close to the processor. Using this memory as shared cache brings novel challenges in resource sharing and request scheduling due to the architectural heterogeneity. This has varied implications on performance of the latency sensitive CPUs vs throughput oriented GPGPUs. The simulations were done on a cycle accurate CPU-GPU simulator (gem5-gpu). Technology used: C/C++, Object orient programming and STLs.

Projects at Samsung R&D

Tizen studio (IDE for Tizen OS) infrastructure development
Tizen Studio is a set of tools for developing Tizen native and Web applications. It consists of an IDE, Emulator and toolchain. It runs on Windows, Ubuntu and macOS. Native applications are developed using the C programming language and are then run on an emulator or a target device.

Analysis and custom implementation of debuggers for tizen applications using Debugger Adapter Protocol for Visual Studio for macOS.
Coaching for professional level internal competitive coding exam on data structures and algorithms

Projects at GOLDMAN SACHS

Re-architecting of resource discovery system

- Technologies used: WPF, WCF, .NET 3.5, SQL Server, IIS7, VS2010
- WPF for the front end with complete MVVM model
- WCF service hosted on IIS7 to act as the model layer
- Framework application to display, store & edit other app config data

Entitlements System

- Technologies used: .NET 3.5, Windows Form, WCF, Windows Service
- Project followed strict OOP principle
- Central system to store the entitlements information for various apps

AngularJS Customization

- Technologies used: AngularJS, Jasmine, REST Service
- Developed custom directives and providers which have a common use case across all the applications (like person lookup)

Framework Library

- Technologies used: Spring, jdk 1.7, Eclipse
- POJO and Spring java client for the various REST services

Inherited several C# projects and was responsible for all the sustenance and continued development / enhancements of the same

Projects at M S Ramaiah Inst of Tech

A comparative Study and Optimization of Hadoop Scheduler [ICECIT 2012]

Hadoop is a general-purpose system that enables high-performance processing of data over a set of distributed nodes. This work focuses on an empirical comparison of the default Hadoop scheduler with Fair scheduler and Capacity scheduler for data intensive applications. We determine suitable schedulers for different class of workloads. Further, we propose improvements over the above schedulers and evaluate the same.

Positions Held

- Teaching Assistant for Compiler Design (E0256,) IISc — Jan 2016 - Apr 2016
- Member of Department Curriculum Committee — 2016 - 2017
- Representative for Student Welfare Committee — 2016 - 2017
- Member of Women in Technology (WiT), Goldman Sachs — 2013 - 2015
- Technology Analyst at Goldman Sachs Nov 2013 - Jul 2015 — Nov 2013 - Jul 2015
- New Analyst Technology Associate at Goldman Sachs — Jun 2012 - Nov 2013

Achievements

- Cleared Samsung Professional level competitive coding exam in first attempt
- Secured distinction in Bharatanatyam Junior Exam (2015)
- Awarded the *"First rank and Gold medal of 2012 batch"* from the Department of Computer Science, M S Ramaiah Institute of Technology.
- Lead the Blood Donation Camp event at MSRIT which achieved the largest volume of blood collected in the Bangalore region (2011)

Co and extra curricular activities

- Routinely performed in dance events including concerts at Ravindra Kalakshetra, Bugle Rock Park Basavanagudi, Our School Auditorium, Banashankari Temple, Sripuram Golden Temple Vellore and Andal Temple Srivilliputhur
- Conducted technology and networking events for Interns at Goldman Sachs (2015)
- Routinely organized activities and events like Blood Donation, notebook drive, school camps for the underprivileged etc, as part of National Service Scheme (NSS) at MSRIT
- Delegated at various conferences and Workshops

Miscellaneous

Languages: English (fluent), Tamil (native), Kannada (native), Hindi (intermediate)

Hobbies:
- An avid classical dance enthusiast and practitioner
- A genuine penchant for reading novels from crime, thriller and drama genre

Other Links: github.com/kumudhan
in.linkedin.com/in/kumudha-narasimhan

References:

Academic References

Dr. Uday Reddy, Guide
Assistant Professor CSA, IISc
uday@iisc.ac.in

Mrs. D S Jayalakshmi, Mentor / Guide
Associate Professor Dept. CSE, MSRIT
jayalakshmids@msrit.edu

Industry References

On Request

Master of Science in Engineering (IISc, Bangalore)

Grades

Course	Grade	Credit
Computer Architecture	A	4
Design and Analysis of Algorithms	B	4
Advanced Compilers	S	4
Final Thesis	In	Progress
	Total	12
	GPA	7.0

Bachelors in Engineering (M S Ramaiah Inst. of Tech, Bangalore)

Principal Courses

- Engineering Mathematics
- Data Structures
- Operating Systems
- Engineering Design
- Web Programming
- Unix System Programming
- Compiler Design
- Discrete Mathematics
- Design & Analysis of Algorithms
- Computer Organization
- Computer Graphics and Visualization
- Advanced Computer Architecture
- Computer Networks
- Software Engineering

Electives

- .NET and C#
- Advanced Mathematics I
- Supply Chain Management
- Advanced Mathematics II

Higher Secondary (Vidya Mandir PU College, PUC Board)

Primary Courses

Physics, Chemistry, Mathematics, Computer Science

Languages in Curriculum

Hindi, English
